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Testing LV PV Inverters Stability during Voltage Magnitude and Vector Shift Disturbances

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Version No.:	2.0
Prepared By:	Panagiotis Bountouris & Dr Ibrahim Abdulhadi
Reviewed By:	Dr Adam Dyśko
Authorised By	Alan Dunn & Dr Federico Coffele
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PROJECT CONTRIBUTORS

The following people contributed to this project:

Scott Wanless

Gordon Jackson

Ronnie Gardiner

DOCUMENT DISTRIBUTION

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EXECUTIVE SUMMARY

This report presents the findings from the physical testing of seven off-the-shelf single and three-phase LV PV inverters carried out at the PNDC. The comprehensive testing that was carried out focused on determining the stability of these inverters during voltage magnitude and vector shift (VS) disturbances that are symptomatic of transmission level faults. The trip/no-trip boundaries for each inverter under test have been recorded. Additional tests have been carried out to determine the stability of these inverters during 50° VS type tests as currently proposed to be included in the G83 recommendation [1]. Unsymmetrical fault conditions have also been simulated and introduced to the three-phase inverters under test.

The test conditions were created using a power electronics based AC grid emulator to which the inverters were connected [2]. The AC grid emulator was controlled in such a way to produce the range of voltage magnitude and VS changes required for the test. Instantaneous voltage and current measurements were taken at the output of the inverters to analyse their response.

The inverters exhibited a wide range of behaviours, however the following key responses have been observed:

- With increasing retained voltage, the inverter is more likely to remain connected with some inverters remaining stable regardless of the retained voltage at a VS of up to ±60°.
- Some inverters will trip at a higher retained voltage threshold when loaded close to their nominal rating.
- The active power output of the inverter is heavily influenced by the retained voltage. At higher retained voltages, the inverters tend to maintain pre-event power output after short transients. Some inverters exhibited a 100% reduction of active power output even at higher retained voltages, but the power would quickly recover after the end of the event. Depending on the penetration level of such inverters and duration of the power loss, this behaviour could potentially lead to momentary loss of significant amount of power, and consequently increase the initial value of RoCoF in the system.
- All inverters remained synchronised to the AC grid emulator during type tests. That is, 50° VS and -50° VS applied from a 49.5Hz and 50Hz initial grid frequency respectively.
- Unsymmetrical faults had a different impact on the two three-phase inverters under test. The 20kW inverter F did not trip on any of the simulated unsymmetrical faults, while the 10kW inverter G tripped for all.

Based on the test results achieved in this project the following key observations follow:

- The wide variety of VS stability limits under different retained voltage conditions indicates that during typical transmission level faults certain amount of inverter connected PV generation may be lost. However, without further analysis of the distribution and penetration levels of various types of inverters in the network it would be very difficult to estimate the potential worst-case scenario.
- The recorded loss of stability at lower retained voltages, often occurring at the voltage step-up (i.e. on fault clearance rather than inception), indicates that the considered G83 type testing procedure performed at nominal voltage (and with no recovery event) may not be sufficient to guard against loss of inverter connected generation during typical transmission system faults. It is believed that some revision of the proposed VS type testing should be considered in discussion with the inverter manufacturers.
- Some of the inverters, while remaining connected, significantly reduce power output during VS and voltage dip events. This effect, even though short in duration (in most cases less than 1 s), may magnify the initial value of system RoCoF during a major system incident (e.g. involving a fault and a loss of major power plant). This in turn can affect the stability of the RoCoF based LOM protection.

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LIST OF ABBREVIATIONS

LV	Low Voltage
PNDC	Power Networks Demonstration Centre
PV	Photovoltaic
RTDS	Real Time Digital Simulator
VS	Vector Shift

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1 INTRODUCTION AND OBJECTIVES

This report presents the findings of the work commissioned by the joint distribution and grid code working group on frequency changes during large disturbances (DC0079). The objective of the work is to experimentally determine the stability of low voltage (LV) photovoltaic (PV) inverters during grid disturbances that impose voltage magnitude and vector shift (VS) changes on the inverter terminals. To achieve this objectives, seven off-the-shelf PV inverters were tested under the aforementioned disturbances using an AC grid emulator at the Power Networks Demonstration Centre (PNDC) [2].

The report is organised as follows. In section 2, a description is provided of the experimental test setup and procedure including the inverters under test, PV emulators that supply DC power to the inverters and a power electronics based system which emulates an AC grid. This is followed by a description of the three test categories considered in this project. The response of each inverter under test is reported in section 3 including a proposed 50° VS type testing procedure. Finally, conclusions are drawn based on the experimental findings.

Due to the large volume of tests carried out, figures and raw measurements associated with each test will be supplied electronically in addition to this report.

2 TEST SETUP AND PROCEDURE

This section describes the test setup used to expose the PV inverters to the voltage disturbances of interest. The tests carried out have been split into three categories as detailed in sections 2.3 – 2.5.

2.1 PV inverters under test

Seven LV PV inverters have been tested during this project. These inverters represent a wide range of manufactures supplying the UK market. The tested inverters are summarised in Table 1.

Table 1. PV inverters under test

Phases	PV Inverter	Rated Active Power	Transformer less[1]	Available Inverter Settings
Single Phase	Inverter A	5kW	Yes	G59/3 [3], G83/2 [1]
	Inverter B	5kW	Yes	G59/3, G83/2
	Inverter C	5kW	No	G59/2 [4], G83/1
	Inverter D	3kW	No	G83/1
	Inverter E	5kW	Yes	G83/2, G59/3
Three Phase	Inverter F	20kW	Yes	G59/3
	Inverter G	10kW	Yes	G59/3, G83/2

In order to supply the inverters under test, two 5kW programmable DC power supplies with PV array emulation have been used. These are the Chroma 62050H-600S and were connected in parallel to provide maximum DC power of 10kW [5]. The maximum open circuit voltage of the PV emulators is 600Vdc. When inputting power into the inverters, this voltage drops to around 480Vdc.

[1] Transformer less PV inverters do not have a built-in isolation transformer at the output.

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The PV emulators can be operated in different modes. However, for the purposes of testing a target power output and maximum DC voltage were set. The PV emulator would then use the built-in EN50530 model to calculate the required current output to enable maximum power point tracking (MPPT) for the inverter [6]. This is deemed sufficient for creating the initial conditions for each test.

2.2 Triphase AC grid emulator

A 540kVA bidirectional converter based programmable power supply manufactured by Triphase was used as an AC grid emulator (see Figure 1) [2]. The unit was controlled to behave as a voltage source that produces the voltage magnitude (nominal voltage of 400V) and phase shifts required for testing. The PV inverters under test were directly connected to the output of the Triphase as shown in Figure 2 and export active power into the Triphase.

A real-time digital simulator (RTDS) [7] was used to produce the reference voltage waveform for the Triphase to reproduce at its output. This reference signal was communicated to the Triphase over a proprietary digital protocol (Aurora Link). Voltage and current measurements at a sampling rate of 5kHz were taken at the output of the PV inverters. The raw data measured during testing is supplied separately both in graphical form and as sampled data stored in CSV text files.

Figure 1. Triphase converter system

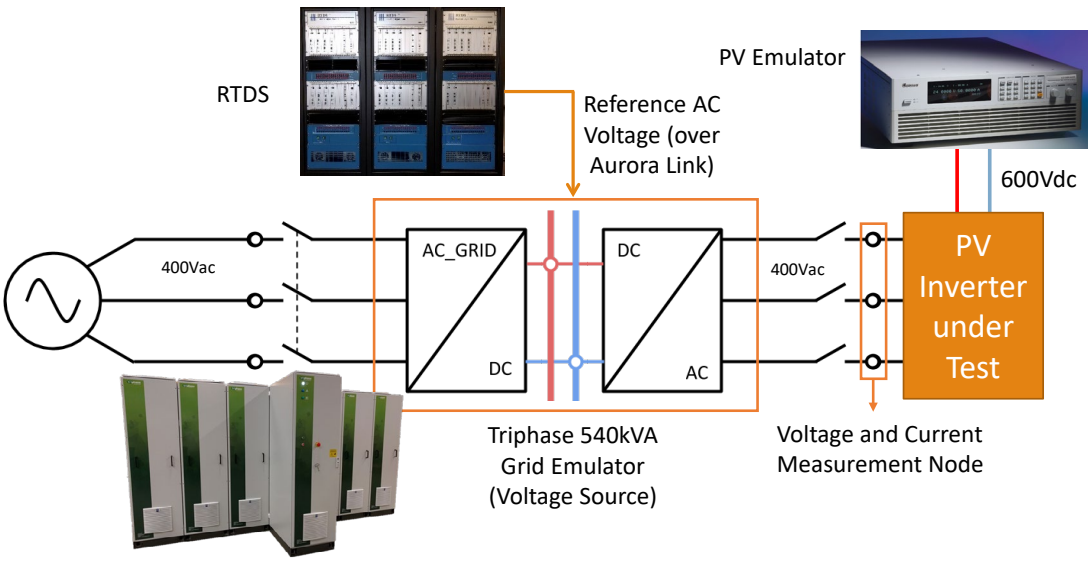

Figure 2. Full test setup configuration.

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NOTE: The three-phase inverters tested require a neutral conductor with a voltage very close to earth potential. The Triphase can be configured with a three-wire or four-wire output. The four-wire-output creates a virtual neutral connection that compensates for imbalances in the circuit. This virtual neutral is actively controlled by the Triphase, so can cause control stability issues when an active system (PV inverter) is connected to it.

To mitigate these issues, a star connected resistive load was connected in parallel with the three-phase inverters under test. The star point was earthed and connected to the inverter neutral conductor so that the inverter neutral potential is tied to earth.

2.3 Test category 1: PV inverter stability during VS and voltage depression events

Test objective: to determine the stability margins of the inverters under voltage depression and VS events.

The specific test configuration used for this category is shown in Figure 3.

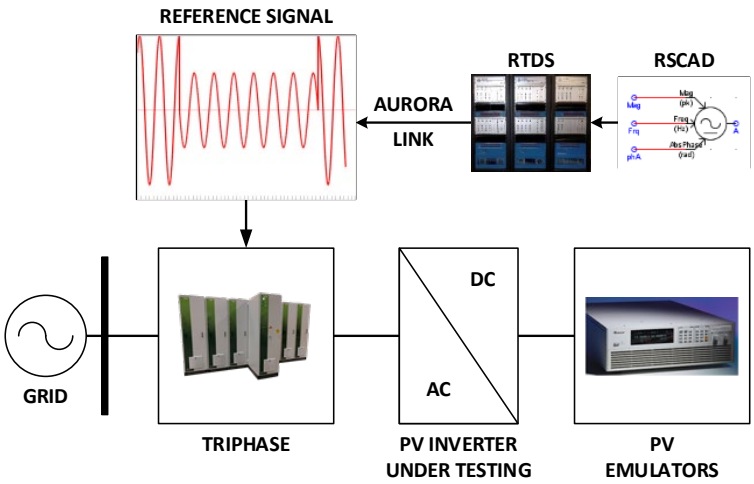

Figure 3. Test configuration for VS and voltage depression tests.

The testing process was carried out as follows:

- Identify the PV inverters stability margin in terms of voltage vector shift (VS) with a simultaneous short-term voltage dip lasting 140 ms (assumed longest transmission level fault clearance time). The retained voltage is systematically reduced in steps of 5% of nominal.
- For each level of retained voltage, a VS is applied starting from 5° and increased in 5° steps, up to 60° or until the inverter trips. The VS and the voltage dip are applied simultaneously, and after 140 ms the same amount of VS angle is introduced in the opposite direction (this opposite VS will be referred to as the recovery VS in this report). This is repeated for negative VS angles. There was no control over the point on wave where the VS was introduced.
- The above steps are performed for inverter loading levels of 50% and 90% of inverter rating where possible.
- A vector shift angle vs. retained voltage characteristic for all inverters is produced showing the trip and no trip margins. These characteristics are presented in section 3.1.
- The inverter is considered stable if it remains connected to the grid for an event that is repeated three times consecutively.

An example voltage waveform showing a -15° VS and 60% retained voltage applied while testing the inverter C is shown in Figure 4. The corresponding measured fundamental frequency VS (derived from a fast Fourier transform - FFT) is shown in Figure 4.

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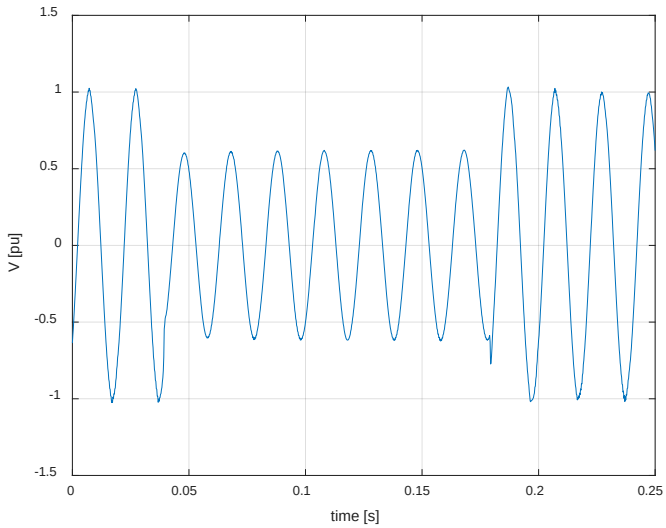

Figure 4. Example waveform showing a -15° VS and 60% retained voltage applied to inverter C.

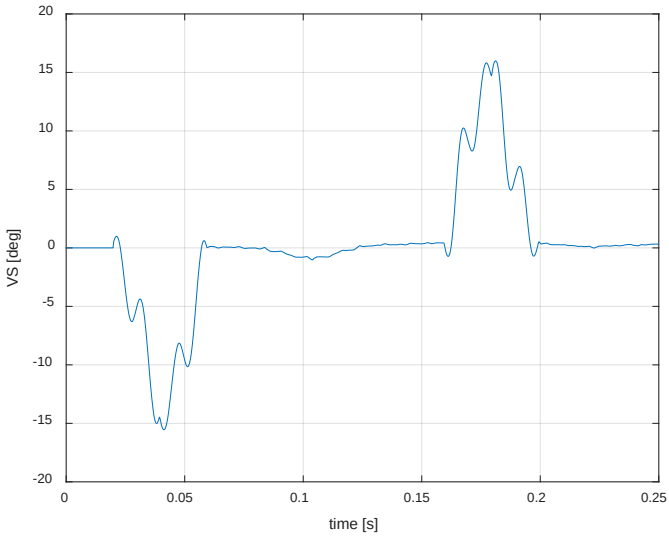

Figure 5. Measured inception and recovery VS for the example waveform in Figure 4.

2.4 Test category 2: PV inverter stability under G83 VS type tests

Test objective: to determine whether the inverters remain synchronised to the grid during a 50° and -50° VS event with an initial grid frequency of 49.5 Hz and 50.5 Hz respectively.

The specific test configuration used for this category is shown in Figure 6. The inverters were loaded up to the maximum possible level prior to the test. In some cases, the maximum achievable power is limited by the PV emulator capacity or when the inverter requires DC input voltage in excess of 480 Vdc to achieve higher power output (which is the case for the three phase inverters).

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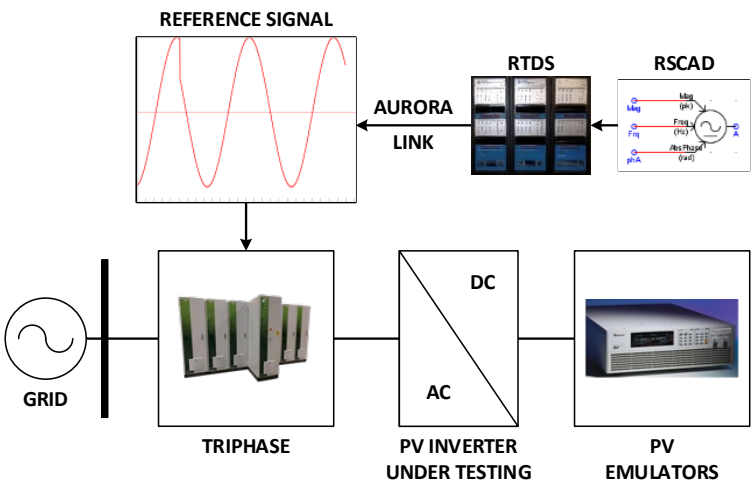

Figure 6. Test configuration for type tests.

The testing process was carried out as follows:

- With a steady state grid frequency of 49.5 Hz and nominal voltage, a single 50° VS is introduced.
- With a steady state grid frequency of 50.5 Hz and nominal voltage, a single -50° VS is introduced.
- Note: No reverse VS angle is applied after the initial VS (in contrast to category 1 tests).

2.5 Test category 3: Three-phase PV inverter stability during unsymmetrical faults

Test objective: to determine whether the three-phase inverters (F and G) remain synchronised to the grid during various unbalanced transmission level faults.

The specific test configuration used for this category is shown in Figure 7. A representative 132kV to LV network has been modelled using typical parameters and transformer winding connection groups. Unsymmetrical faults were introduced at the 132kV level, while the resulting LV voltages (where an LV inverter would be connected) were recorded and used as the reference waveform for the Triphase system to reproduce at its output. A single line diagram of the modelled transmission/distribution circuit is shown in Figure 8, and a screenshot of the circuit modelled in RTDS/RSCAD is shown in Figure 9.

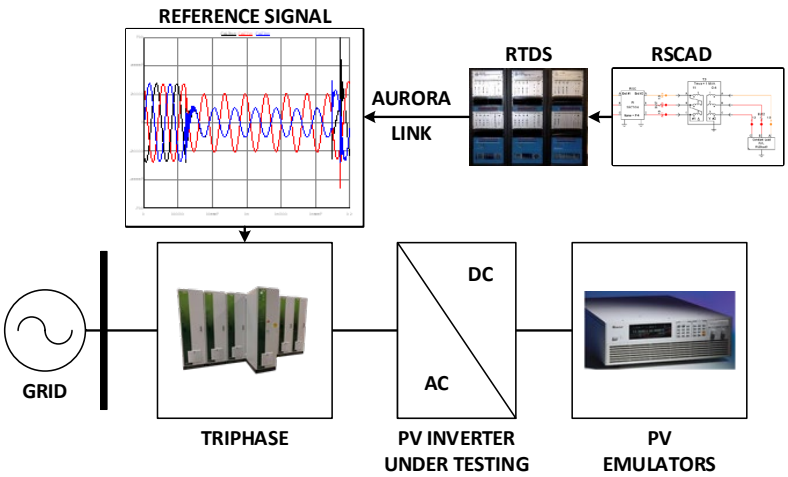

Figure 7. Test configuration for unsymmetrical transmission level faults.

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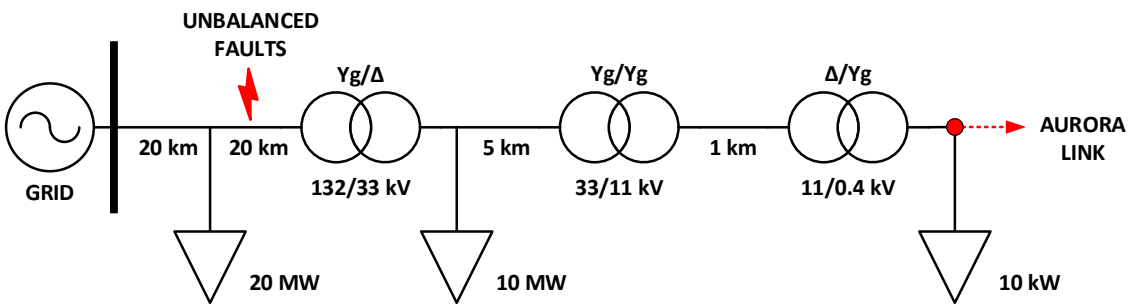

Figure 8. Single line diagram of the test circuit for unsymmetrical faults.

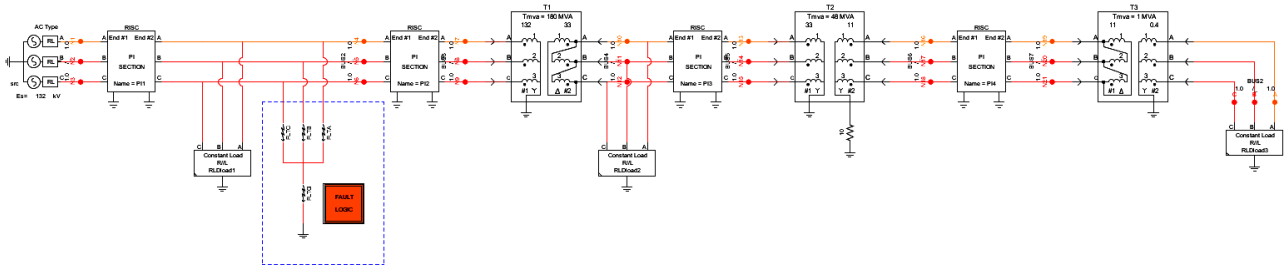

Figure 9. RSCAD model of the test circuit for unsymmetrical faults.

The main parameters of the modelled test network are summarised in Table 2 and Table 3:

Table 2. Transformer parameters

Element	Voltage (kV)	Capacity (MVA)
Transformer 1	132/33	180
Transformer 2	33/11	48
Transformer 3	11/0.4	1

Table 3. Line parameters

Power Lines (represented as PI sections)	PI section 1	PI section 3	PI section 4
Voltage (kV)	132	33	11
Length (km)	40	5	1
Positive/zero sequence resistances (Ω/km)	0.01273/0.3864	0.01273/0.3864	0.01273/0.3864
Positive/zero sequence inductances (mH/km)	0.9337/4.1264	0.9337/4.1264	0.9337/4.1264
Positive/zero sequence capacitances (µF/km)	12.74/7.751	12.74/7.751	12.74/7.751

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The following unsymmetrical faults were applied: phase-to-ground, two-phase-to-ground, and phase-to-phase. Both solid faults and resistive 1Ω faults were applied. The duration of each fault was 140 ms. When testing the three-phase inverter G, 10Ω and 20Ω fault resistance were also applied to determine if an increased retained voltage improves the inverter stability during unsymmetrical faults.

3 SUMMARY OF TEST RESULTS AND MAIN OBSERVATIONS

This section presents the main inverter responses and characteristics for each test category. Due to large volume of data a complete set of key measurements are provided separately, both as time domain graphs (emf and jpg graphical files), and as raw sampled data (csv comma separated files). The supplied plots include for each inverter the following signals (both for trip and no trip responses):

- Inverter RMS voltage.
- Inverter RMS current.
- Measured VS using FFT and one-cycle window.
- Exported real and reactive power, where a positive value signifies export from the inverter and a negative value signifies import into the inverter.

The VS response characteristics presented in this section use the assumed VS as set in the RTDS reference simulation. However, an empirical assessment has also been performed to evaluate the errors introduced by the Triphase system. It was observed that these errors are typically larger when the retained voltage is low as the waveform is more easily distorted. Table 4 illustrates some of these errors for a few selected test cases. As the error was observed to be within the 5° VS step in the vast majority of cases (especially at the higher retained voltages) it was deemed acceptable for the purposes of this test.

Table 4. Example errors in applied VS

Test case	Assumed inception VS	Measured inception VS	Error	Assumed Recovery VS	Measured Recovery VS	Error
Inverter B, 50% loading, 95% retained voltage	60°	57.78°	2.22°	-60°	-58.22°	1.78°
Inverter C, 50% loading, 10% retained voltage	-50°	-43.25°	6.75°	50°	45.86°	4.14°
Inverter E, 90% loading, 50% retained voltage	-60°	-56.51°	3.49°	60°	59.95°	0.05°

3.1 Test category 1

The voltage magnitude and VS stability boundaries identified for all inverters under test are presented here using a stable/unstable VS characteristic for each retained voltage value between 5% and 100%. The observed response of the inverter during a 0% retained voltage event (no VS applicable) is stated separately and also summarised in Table 5. A separate characteristic is presented for each tested loading level where applicable.

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Table 5. Response of Inverters under 0% retained voltage test

Inverter	A	B	C	D	E	F	G
Trip at 0% retained voltage	N	Y	N (50% loading), Y (80% loading)	Y	Y	N	N

3.1.1 Single-phase 5 kW inverter A

Figure 10 and Figure 11 show that the inverter A does not trip for a VS of up to ±60° for all retained voltages between 5% and 100%, including both 50% and 90% loading conditions. The inverter also does not trip at 0% retained voltage.

The output power will vary based on the retained voltage. The inverter attempts to maintain pre-event active power output after a short transient. Active power recovery after severe voltage depressions normally occurs immediately after the end of the 140 ms event. An example of this is shown in Figure 12.

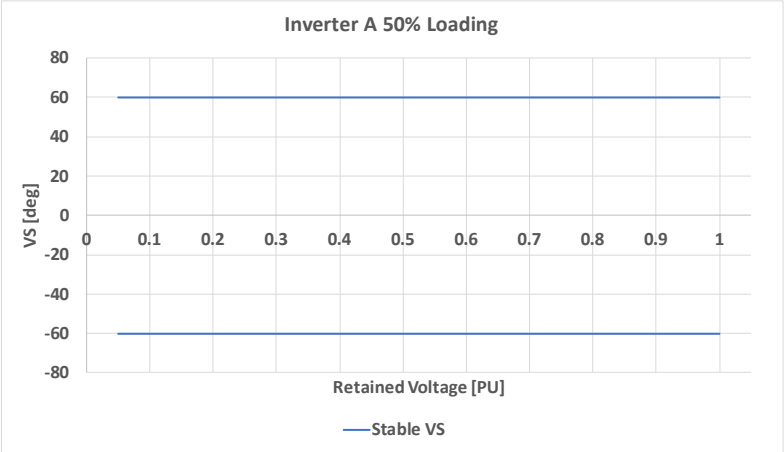

Figure 10. Inverter A stability characteristic at 50% loading

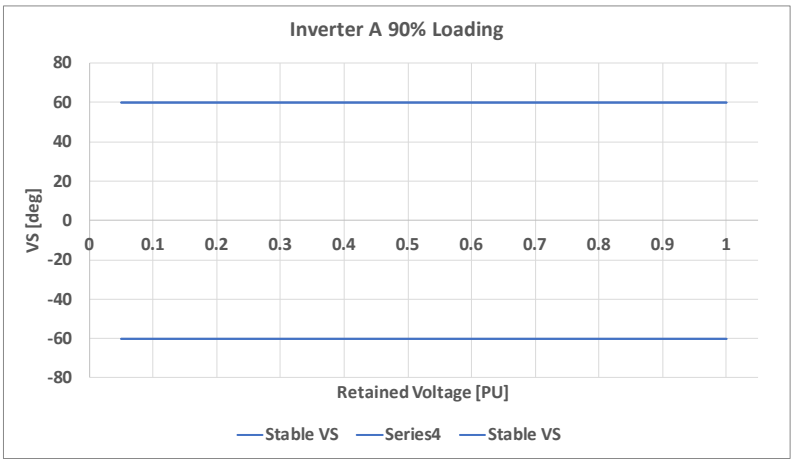

Figure 11. Inverter A stability characteristic at 90% loading

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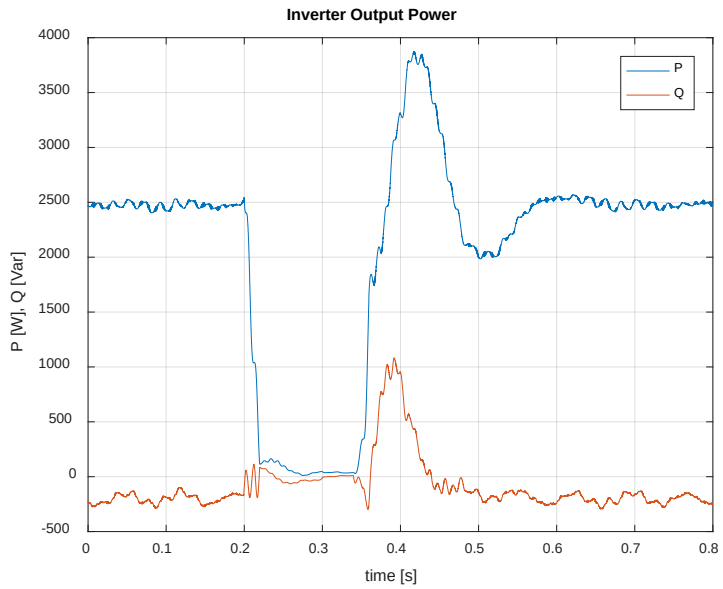

Figure 12. Inverter A output power during a 60° VS, 5% retained voltage event

3.1.2 Single-phase 5kW inverter B

Figure 13 and Figure 14 show that the single-phase 5kW inverter B trips for events with a retained voltage of 65% and below (including 0%) without a VS applied. However, the inverter does not trip for ±60° VS events at 75% or higher retained voltages and both 50% and 90% loading levels.

At a 70% retained voltage, even when the inverter does not trip, the output active power has been observed to temporarily drop to zero and recover after the end of the test event (as shown in Figure 15). At higher retained voltages, the inverter attempts to maintain the pre-event output power after a short transient.

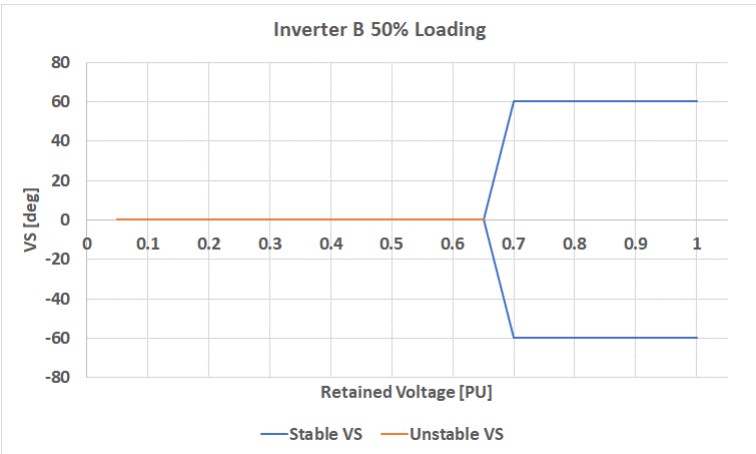

Figure 13. 5kW inverter B stability characteristic at 50% loading

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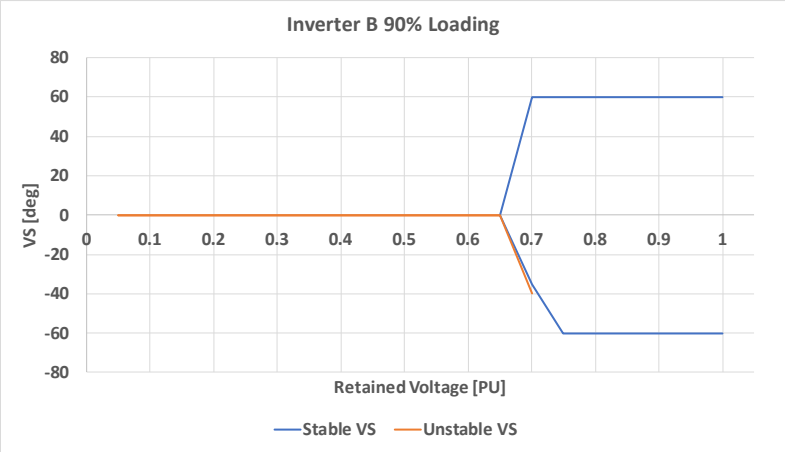

Figure 14. 5kW inverter B stability characteristic at 90% loading

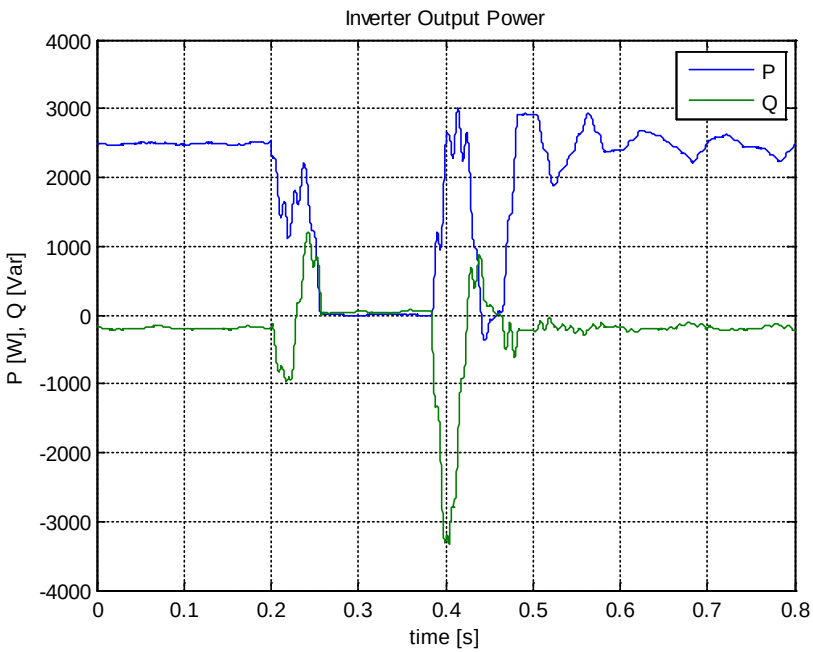

Figure 15. 5kW inverter B output power during a -60° VS, 70% retained voltage event

3.1.3 Single-phase 5kW inverter C

Figure 16 and Figure 17 show the stable and unstable VS boundaries for the inverter C. The inverter remains stable for relatively higher VS under retained voltages over 80% compared to lower retained voltages. When the inverter is loaded at 50%, it also exhibits relatively high VS stability at retained voltages between 5% and 15%, compared to when it is loaded at 80% where it trips for these retained voltage levels with no VS applied. At 0% retained voltage, the inverter does not trip at 50% loading, but trips at 80% loading. Similar to other inverters, the active power output changes depending on the retained voltage as shown in Figure 18.

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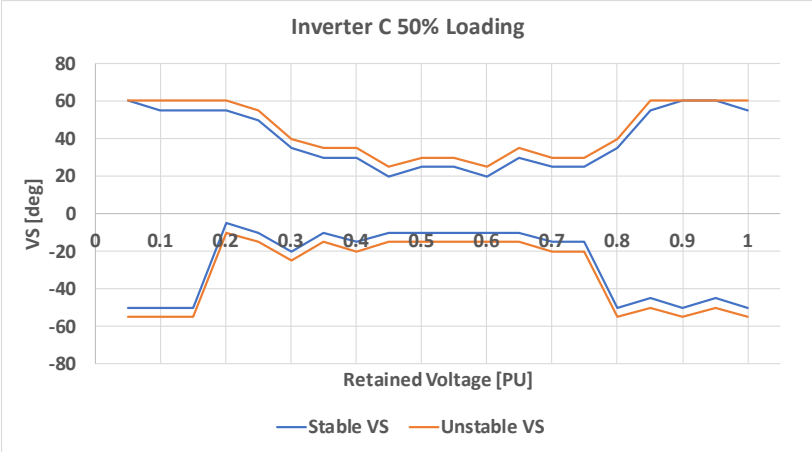

Figure 16. 5kW inverter C stability characteristic at 50% loading

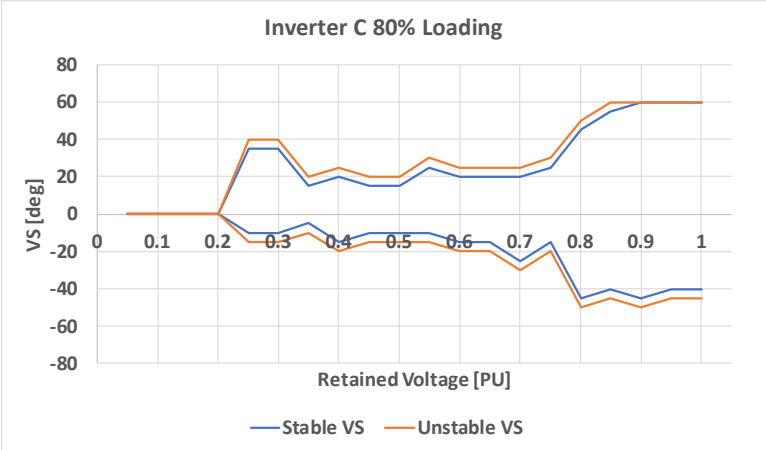

Figure 17. 5kW inverter C stability characteristic at 80% loading

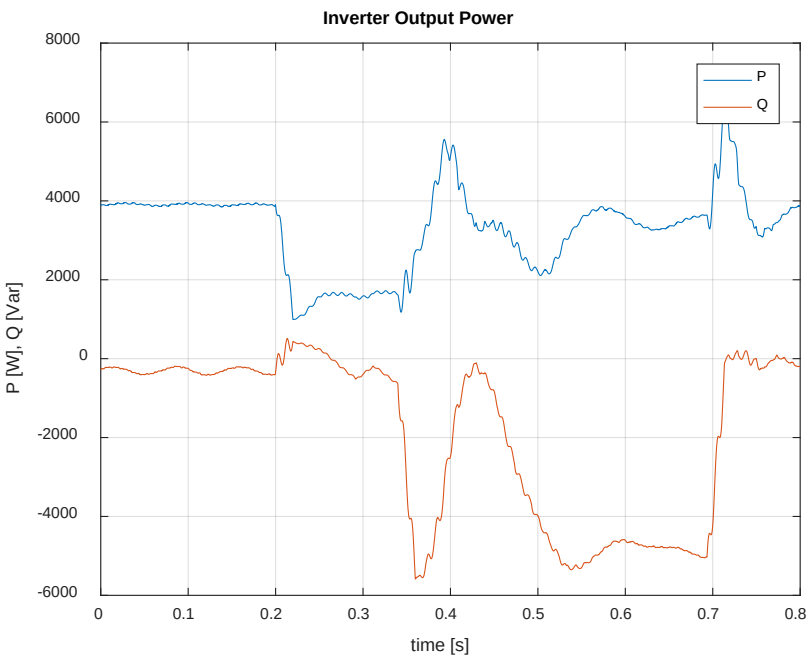

Figure 18. 5kW inverter C output power during a 35° VS, 25% retained voltage event

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3.1.4 Single-phase 3kW inverter D

Figure 19 and Figure 20 show the stability characteristics for the single-phase inverter D. The characteristics are fairly similar with the inverter tripping for a 20% and below retained voltage event without a VS being applied when it is loaded at 50%. At a higher loading of 90%, the inverter trips at 35% retained voltage without a VS being applied. In both loading cases, the inverter trips at 0% retained voltage.

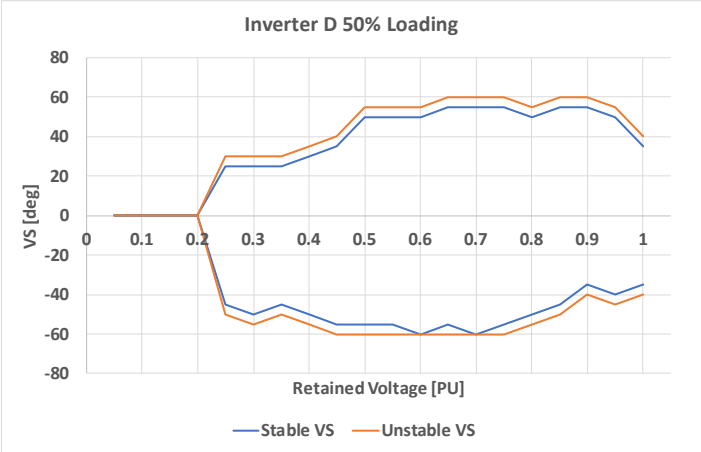

Figure 19. 3kW inverter D stability characteristic at 50% loading

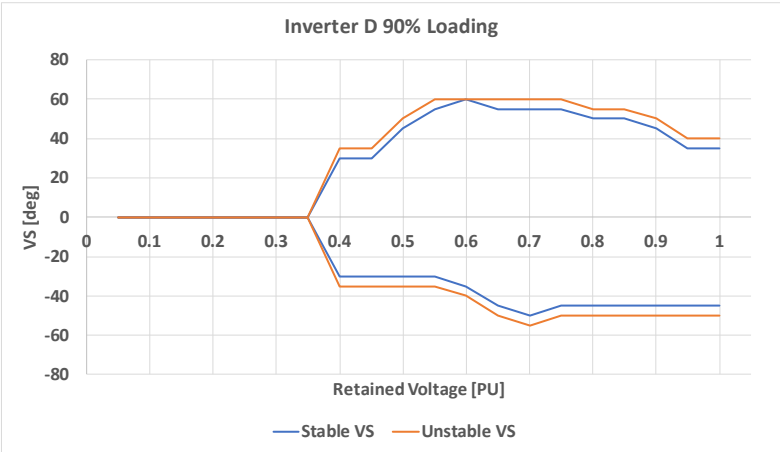

Figure 20. 3kW inverter D stability characteristic at 90% loading

3.1.5 Single-phase 5kW inverter E

Figure 21 and Figure 22 show the stability boundaries for inverter E. In both loading cases, the inverter trips at retained voltages below 15% without a VS being applied. Between 20% and 30% retained voltages, the inverter remains stable for a relatively high VS, but the behaviour is not necessarily consistent with higher retained voltages as the characteristics show.

The inverter active power output varies with the retained voltage. Under certain test conditions, the inverter has been observed to absorb active power for trip and no trip responses as depicted in Figure 23 and Figure 24 respectively. Furthermore, active power recovery after the event can be relatively slower (ramped) compared to inverter A, for instance, as can be seen in Figure 24.

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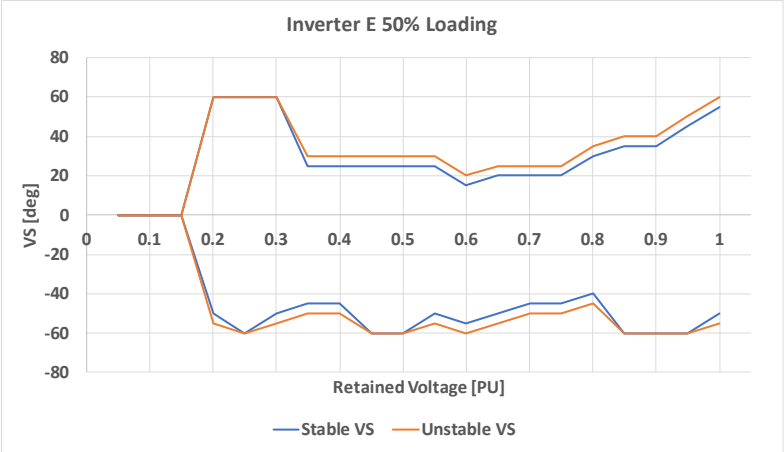

Figure 21. 5kW inverter E stability characteristic at 50% loading

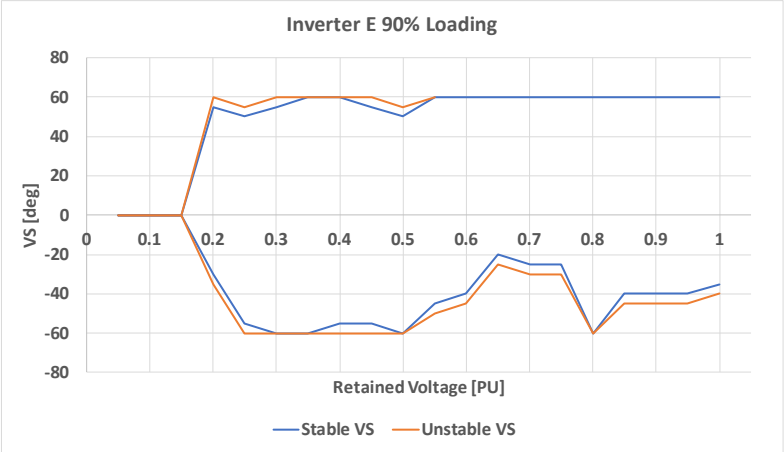

Figure 22. 5kW inverter E stability characteristic at 90% loading

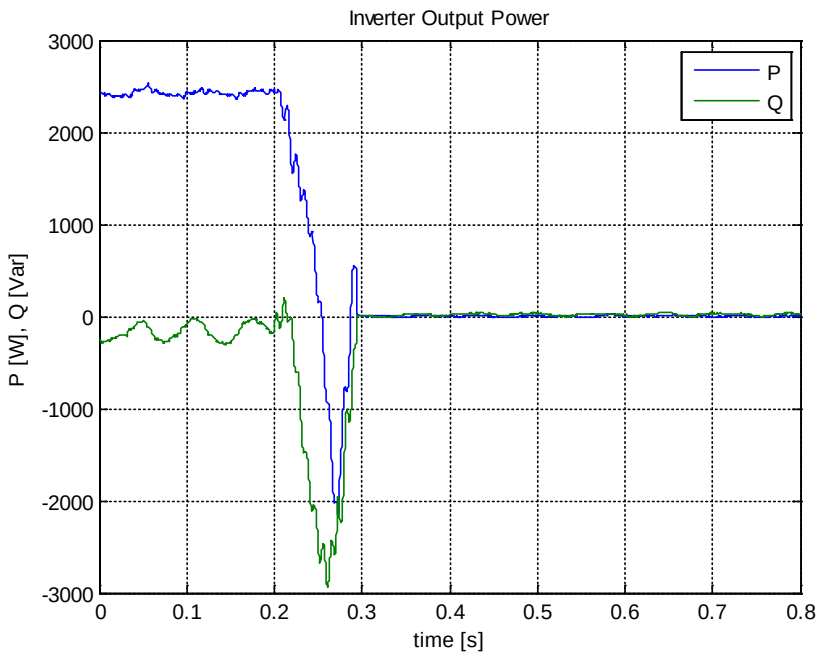

Figure 23. 5kW inverter E absorbing active power during a 20° VS, 60% retained voltage event

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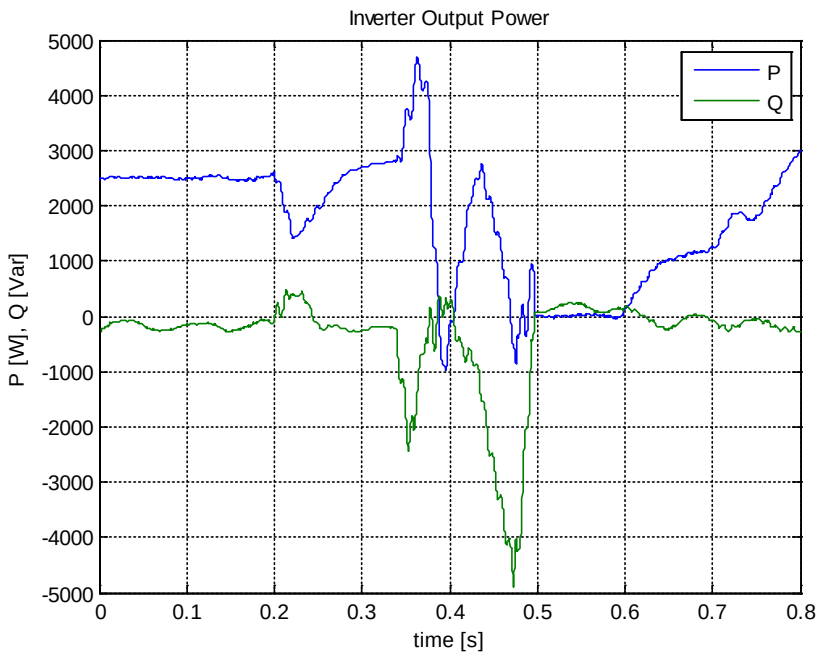

Figure 24. 5kW inverter E absorbing active power during a 25° VS, 45% retained voltage event

3.1.6 Three-phase 20kW inverter F

Figure 25 shows that the three-phase inverter F does not trip for VS of up to ±60° for retained voltages between 5% and 100%. The inverter does not trip at 0% retained voltage either. The maximum loading level achieved with this inverter was 30% (6kW), due to the relatively low DC voltage supplied by the PV emulators compared to that required for a higher power output by three phase inverters.

A transient reduction in active power can be observed during the inception and recovery VS at higher retained voltages. An example of this is shown in Figure 26.

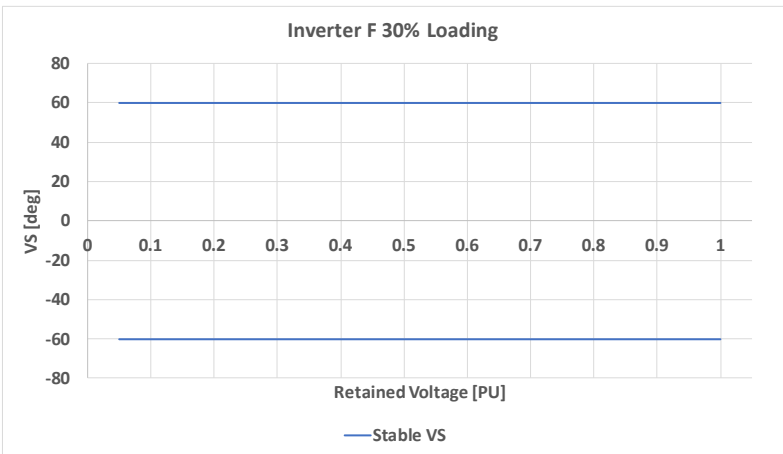

Figure 25. 20kW three-phase inverter F stability characteristic at 30% loading

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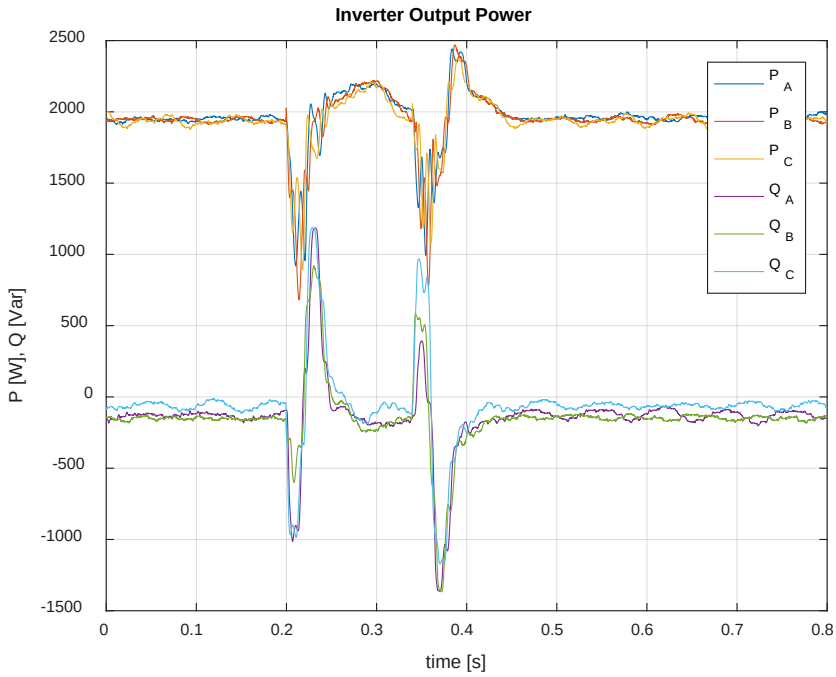

Figure 26. 20kW three-phase inverter F output power during a -60° VS, 100% retained voltage event

3.1.7 Three-phase 10kW inverter G

Figure 27 shows that the three-phase inverter G does not trip for VS of up to ±60° for retained voltages between 5% and 100%. The inverter also does not trip at 0% retained voltage. Similar to the three-phase inverter F, a maximum loading of 30% was achieved.

There is no notable behaviour regarding the power output, where it is generally reduced with higher voltage depressions and can decrease to zero for the duration of the 140 ms event, followed by a power output recovery as shown in Figure 28.

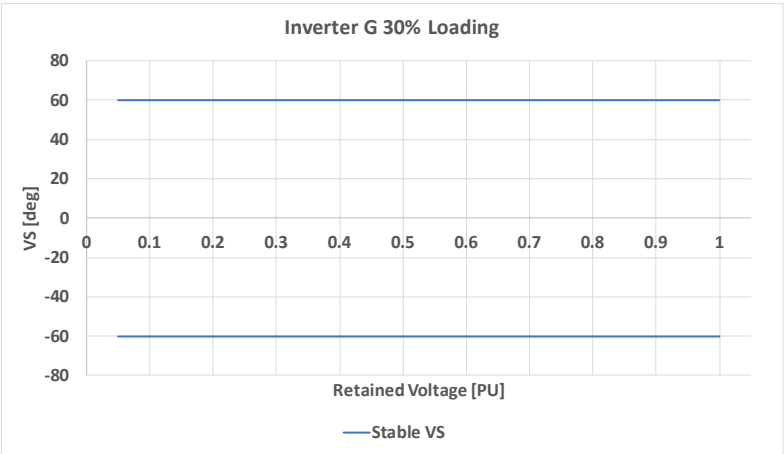

Figure 27. Three-phase 10kW inverter G stability characteristic at 30% loading

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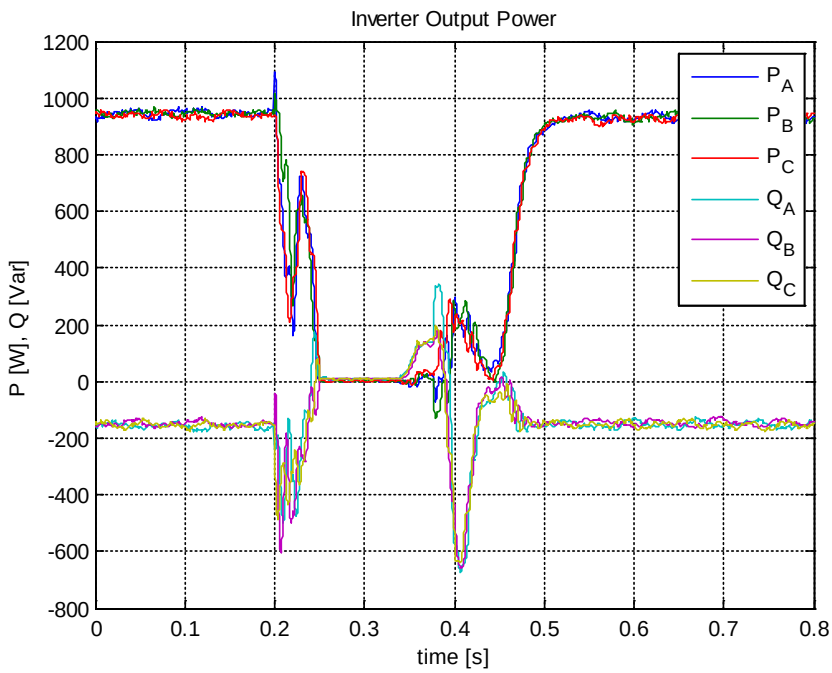

Figure 28. 10kW three-phase inverter G output power during a -60° VS, 25% retained voltage event

Finally, inverter tripping has been observed to occur on either the inception of the VS or the recovery VS.

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3.2 Test category 2

Table 6 summarises the response of the inverters during this test category (G83 recommended VS type testing) along with the initial loading and grid frequency. None of the inverters tripped during the tests. It is worth noting that the single-phase inverter D is an older unit with only G83/1 settings. This means that over frequency protection would operate at 50.5 Hz. Therefore, the type test with an initial frequency of 50.5Hz was not applied to this inverter.

Table 6. Summary of inverter performance during type testing

Inverter	Trip	Loading	Retained Voltage [%]	Initial Frequency [Hz]	Vector Shift [deg]
1 ph - A	N	100%	100	49.5	50
	N	100%	100	50.5	-50
1 ph - B	N	100%	100	49.5	50
	N	100%	100	50.5	-50
1 ph - C	N	80%	100	49.5	50
	N	80%	100	50.5	-50
1 ph - D	N	100%	100	49.5	50
1 ph - E	N	100%	100	49.5	50
	N	100%	100	50.5	-50
3ph - F	N	30%	100	49.5	50
	N	30%	100	50.5	-50
3 ph - G	N	30%	100	50.5	50
	N	30%	100	49.5	-50

3.3 Test category 3

This test category was applied only to the three-phase inverters (F and G) while loaded at 30%. Inverter F did not trip for any of the unsymmetrical faults, while inverter G tripped for all unsymmetrical faults. Following this outcome, the fault resistances were increased to 10Ω and 20Ω and the tests repeated for inverter G to determine whether the higher resulting retained voltage would improve the inverter stability. Inverter G, however, also tripped for all unsymmetrical faults with the higher fault resistance.

A maximum VS of around 65° VS was observed when an A-B-G solid fault was applied to both inverters. A maximum voltage drop of around 80% on the B phase has been observed during this test. The measured voltage and power output of both inverters during this event are shown in Figures 29 to 32.

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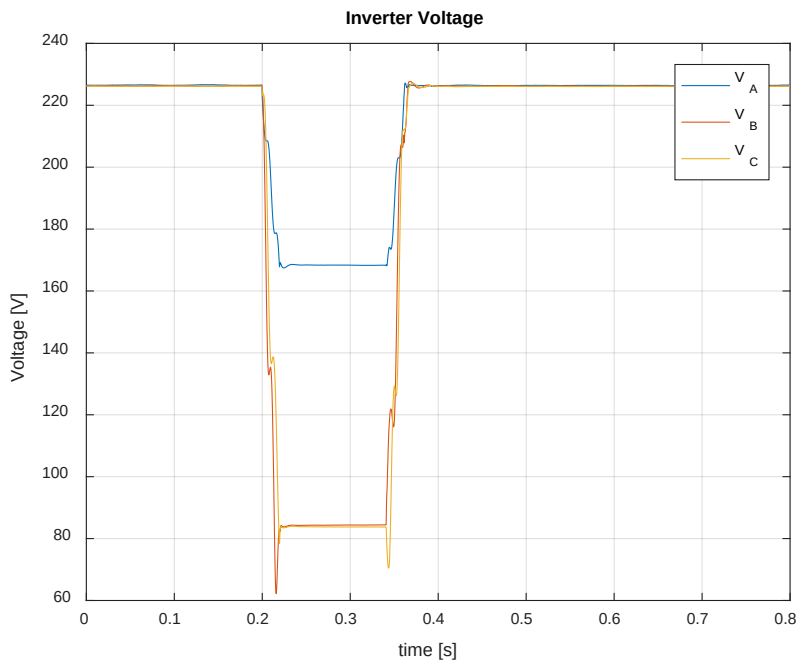

Figure 29. 20kW inverter F voltage during a solid A-B-G fault applied to the 132kV circuit

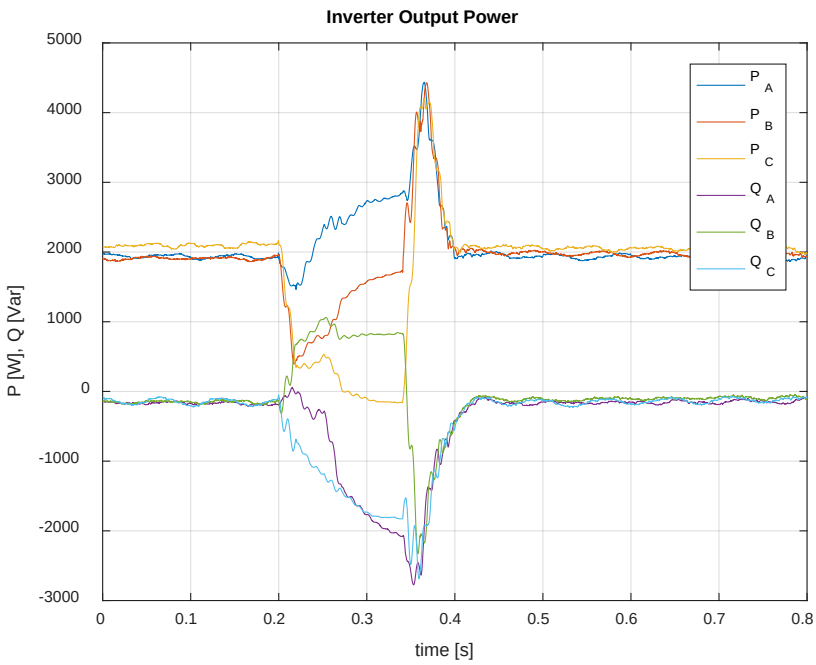

Figure 30. 20kW inverter F output power during a solid A-B-G fault applied to the 132kV circuit

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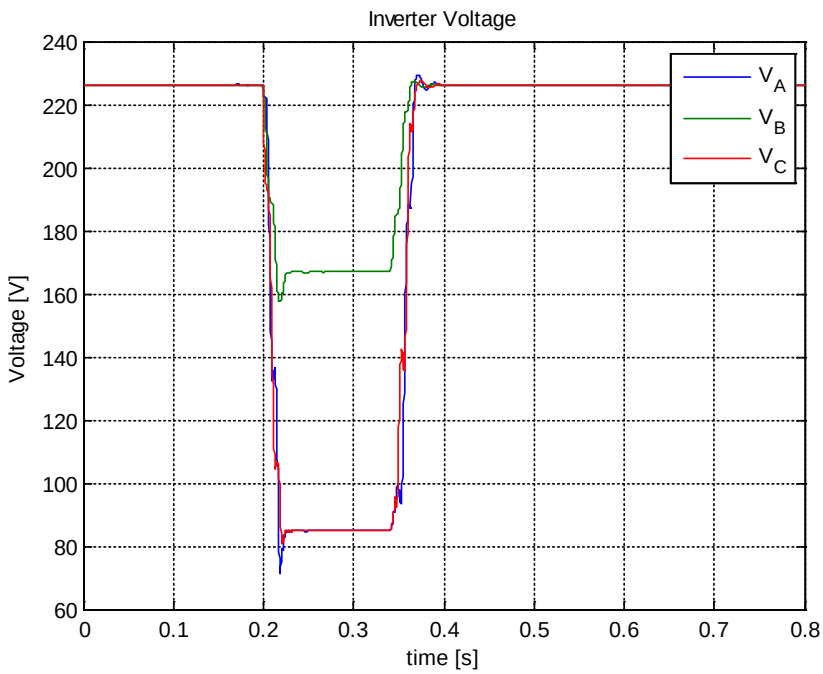

Figure 31. 10kW inverter G voltage during a solid A-B-G fault applied to the 132kV circuit

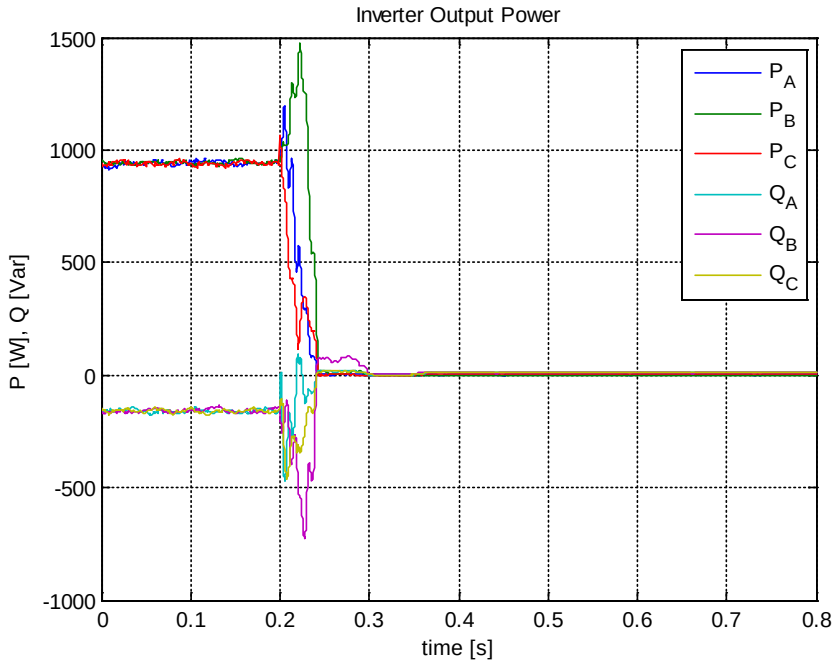

Figure 32. 10kW inverter G output power during a solid A-B-G fault applied to the 132kV circuit

It is thought that the inverter G tripping was caused by a negative sequence based protection. To verify this, two additional tests were performed, both of which apply negative sequence voltage to the inverter output:

- A vector shift of 50° was applied for 140 ms to one of the phases without a reduction in voltage magnitude.
- A step reduction in voltage to 70% retained was applied for 140 ms to one of the phases without a vector shift.

The inverter tripped for both of these events. Figure 33 to Figure 36 illustrate the additional tests applied and the resulting inverter response.

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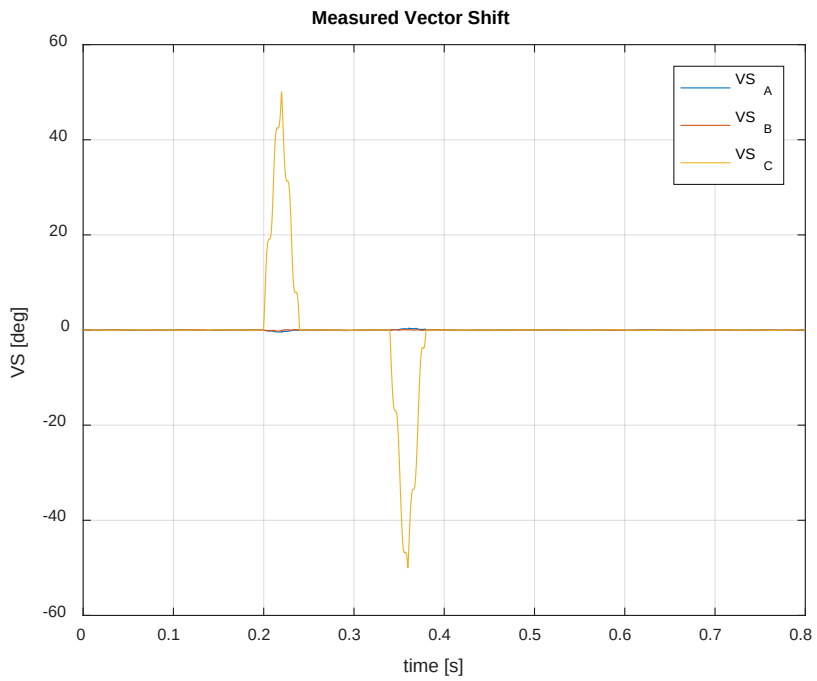

Figure 33. 50° VS applied to phase C of the three-phase inverter G

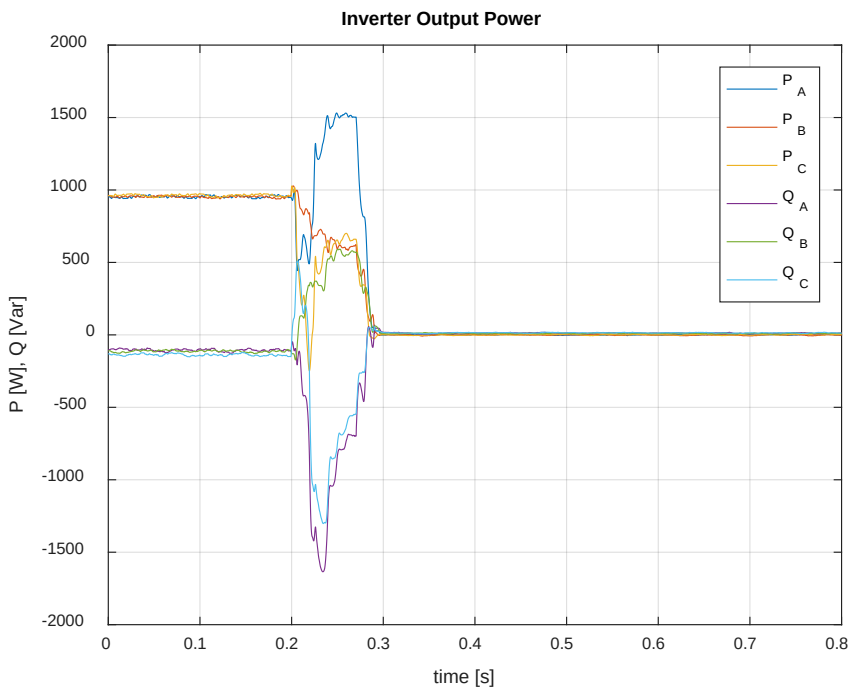

Figure 34. Inverter G output power after the application of a 50° VS on phase C

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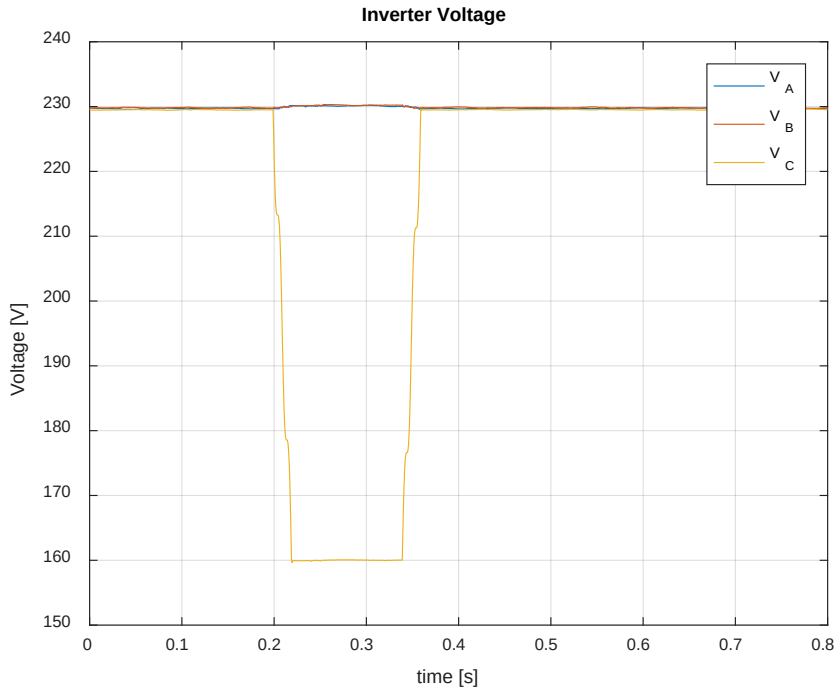

Figure 35. 30% voltage magnitude reduction applied to phase C of the three-phase inverter G

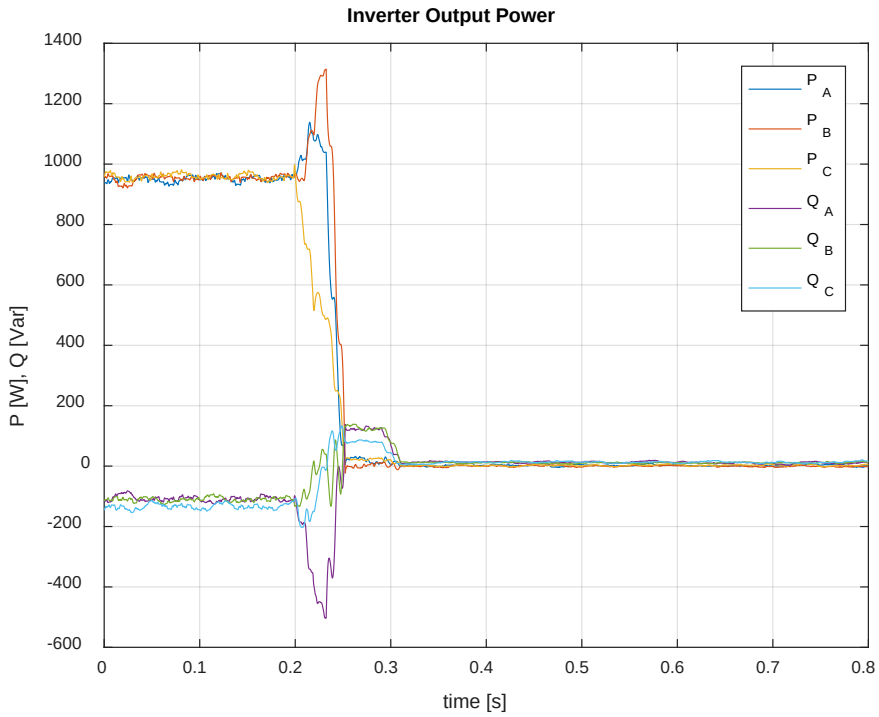

Figure 36. Inverter G output power after the application of 30% voltage magnitude reduction on phase C

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4 SUMMARY AND KEY FINDINGS

Seven off-the-shelf single-phase and three-phase LV PV inverters have been tested for stability under the following range of conditions:

1. Simultaneous voltage magnitude and VS disturbances where the stability margins have been quantified up to ±60° VS in 5° increments and between 0% - 100% retained voltage in 5% increments. Where possible two inverter loading levels were also considered. The test events had a fixed duration of 140 ms followed by the VS angle shift in the opposite direction and restoration of the voltage magnitude to nominal.
2. A 50° VS type test (proposed for G83) was applied to all single-phase inverters.
3. Unsymmetrical solid and resistive (1Ω, 10Ω, 20Ω) faults with a fixed duration of 140 ms were applied to the three-phase inverters under test.

The inverters have exhibited a wide range of behaviour under the voltage magnitude and VS disturbance tests, but the following salient characteristics have been observed:

- **Single-phase 5kW inverter A**: did not trip for any VS events up to ±60° and all retained voltage levels down to 0%. Reduction in active power that is mostly driven by the voltage reduction has been observed. The inverter quickly recovers its pre-event power output after the event ends.
- **Single-phase 5kW inverter B**: did no trip for VS events up to ±60° as long as the retained voltage is above 75%. The inverter trips when the retained voltage is below 65% without a VS being applied regardless of inverter loading. At 70% retained voltage, the inverter has been observed to reduce its active power output to zero and recover after the event ends. Otherwise, the inverter attempts to maintain pre-event active power output.
- **Single-phase 5kW inverter C**: the inverter is generally more stable at higher retained voltages and more so with positive VS angle events. At a higher loading of 80%, the inverter trips at retained voltages of 20% and below. Similar to other inverters, the active power output during an event depends on the retained voltage.
- **Single-phase 5kW inverter E**: trips without a VS being applied for retained voltages of 15% and below. The stability boundary then is heavily dependent on the VS and retained voltage level above 15%. The inverter has been observed to absorb active power during some of the test events.
- **Single-phase 3kW inverter D**: the inverter is generally more stable at higher retained voltages. At 50% loading, the inverter trips with no VS applied at retained voltages of 20% and below, while at 90% loading, the threshold is increased to 35% retained voltage and below.
- **Three-phase 20kW inverter F**: did not trip for any VS events up to ±60° and all retained voltage levels down to 0% for a 30% loading level. Active power output can be reduced during voltage depressions, as is the case with all the inverters.
- **Three-phase 10kW inverter G**: did not trip for any VS events up to ±60° and all retained voltage levels down to 0% for a 30% loading level. Active power output can be reduced during voltage depressions, as is the case with all the inverters.

All inverters remained stable (i.e. did not trip) during the 50° VS type test. It is worth noting though that the type test does not specify a recovery VS event angle after 140 ms as applied in the first set of VS tests. The recovery VS has been the cause of some inverters to trip during the VS tests rather than the first inception of the VS event.

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The impact of unsymmetrical solid and resistive faults applied at a simulated 132kV network and the resulting LV voltage depression and VS seen by the three-phase inverters under test was determined. The 20kW inverter F, loaded at 30%, did not trip for any of the unsymmetrical faults. In contrast, the inverter G, loaded at 30%, tripped for all unsymmetrical fault tests. The maximum VS observed during these tests was around 65° at a maximum voltage depression of around 80% on the B phase during a solid A-B-G fault.

Based on the LV inverter test results achieved in this project the following key observations and recommendations follow:

- The wide variety of VS stability limits under different retained voltage conditions indicates that during typical transmission level faults certain amount of inverter connected PV generation may be lost. However, without further analysis of the distribution and penetration levels of various types of inverters in the network it would be very difficult to estimate the potential worst-case scenario.
- The recorded loss of stability at lower retained voltages, often occurring at the voltage step-up (i.e. on fault clearance rather than inception), indicates that the considered G83 type test procedure performed at nominal voltage (and with no recovery event) may not be sufficient to guard against loss of inverter connected generation during typical transmission system faults. It is believed that some revision of the proposed VS type testing should be considered in discussion with the inverter manufacturers.
- Some of the inverters, while remaining connected, significantly reduce power output during VS and voltage dip events. This effect, even though short in duration (in most cases less than 1 s), may magnify the initial value of system RoCoF during a major system incident (e.g. involving a fault and a loss of major power plant). This in turn can affect the stability of the RoCoF based LOM protection.

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